IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: LEE, YONG-UK ET AL.	)	
	)	Group Art Unit: 2629
Serial No.: 10/829,294	)	
	)	
Filed: April 22, 2004	)	Examiner:
	)	ABDULSELAM, ABBAS I.
For: ELECTROPHORETIC DISPLAY DEVICE	)	
	)	Confirmation No. 7218

REPLY TO NON-FINAL OFFICE ACTION
UNDER 37 C.F.R. § 1.111, WITH AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants respectfully request entry of the following amendments and remarks contained herein in response to the Office Action mailed November 20, 2007. Applicants respectfully submit that the amendments and remarks contained herein place the instant application in condition for allowance.

Amendments to the claims are reflected in the listing of claims, which begins on page 2 of this paper; and

Remarks begin on page 8 of this paper.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (Currently amended) An electrophoretic display comprising:

a gate line which extends in a first direction;

a data line which extends in a second direction substantially perpendicular to the first direction;

a first pixel electrode ~~overlapping one of the gate line and the data line~~disposed in a first region restricted by the gate line and the data line; and

a second pixel electrode ~~overlapping the one of the gate line and the data line~~disposed in a second region restricted by the gate line and the data line and disposed adjacent to the first region,

wherein ~~the first pixel electrode and the second pixel electrode overlap a same gate line or data line and are separated by a predetermined distance~~ one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode.

2. (Currently amended) The electrophoretic display of claim 1, wherein ~~a portion~~ the portion of the first pixel electrode and ~~a portion~~ the portion of the second pixel electrode overlap a portion of a width of the data line extending in the second direction between adjacent gate lines.

3. (Previously presented) The electrophoretic display of claim 1, further comprising:

an insulating layer interposed between the data line and one of the first pixel electrode and the second pixel electrode,

wherein the insulating layer has a dielectric constant lower than 4.

4. (Previously presented) The electrophoretic display of claim 1, wherein the data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti.

5. (Previously presented) The electrophoretic display of claim 1, further comprising:

a thin film transistor comprising:

a channel;

a source electrode; and

a drain electrode;

wherein the first pixel electrode and the second pixel electrode are made of opaque material, and

wherein the first pixel electrode and the second pixel electrode overlap the channel of the thin film transistor.

6. (Previously presented) The electrophoretic display of claim 3, wherein the insulating layer is made of a-Si:C:O or a-Si:O:F.

7. (Currently amended) An electrophoretic display comprising:

a substrate;

a gate line which extends in a first direction; and

a data line which extends in a second direction substantially perpendicular to the first direction;

a first thin film transistor comprising:

a first channel;

a first gate electrode;

a first source electrode;

a first drain electrode; and

a first semiconductor ~~layer,~~ layer;

~~an opaque layer~~ a first opaque layer formed on the first semiconductor layer and disposed over the channel of the first thin film transistor;

a second thin film transistor disposed adjacent to the first thin film transistor and comprising:

a second channel;

a second gate electrode;

a second source electrode;

a second drain electrode; and

a second semiconductor layer;

a second opaque layer formed on the second semiconductor layer and disposed over the channel of the second thin film transistor;

a first pixel electrode ~~overlapping one of the gate line and the data line~~ disposed over the first thin film transistor; and

a second pixel electrode ~~overlapping the one of the gate line and the data line~~ disposed over the second thin film transistor,

wherein ~~the first pixel electrode and the second pixel electrode overlap a same gate line or data line and are separated by a predetermined distance~~ one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode.

8. (Canceled)

9. (Previously presented) The electrophoretic display of claim 7, further comprising:

an insulating layer formed between the data line and one of the first pixel electrode and the second pixel electrode,

wherein the insulating layer has a dielectric constant smaller than 4.

10. (Previously presented) The electrophoretic display of claim 7, wherein the data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti.

11. (Previously presented) The electrophoretic display of claim 7,

wherein the first pixel electrode and the second pixel electrode are made of opaque material, and

wherein the first pixel electrode and the second pixel electrode overlap the channel of the thin film transistor.

12. (Previously presented) The electrophoretic display of claim 9, wherein the insulating layer is made of a-Si:C:O or a-Si:O:F.

13. (Canceled)

14. (Currently amended) An electrophoretic display comprising:

~~a substrate; and~~ substrate;

a thin film transistor formed on a surface of the substrate, the thin film transistor comprising:

a source electrode and a drain electrode formed on the substrate;

a semiconductor layer formed on the source electrode and the drain electrode;

an insulation layer formed on the semiconductor layer; and

a gate electrode formed on the insulation layer;

a gate line which extends in a first direction;

a data line which extends in a second direction substantially perpendicular to the first direction;

a first pixel electrode ~~overlapping one of the gate line and the data line~~disposed in a first region restricted by the gate line and the data line; and

a second pixel electrode ~~overlapping the one of the gate line and the data line~~disposed in a second region restricted by the gate line and the data line and disposed adjacent to the first region,

wherein ~~the first pixel electrode and the second pixel electrode overlap a same gate line or data line and are separated by a predetermined distance~~ one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode.

15. (Canceled)

16. (Previously presented) The electrophoretic display of claim 14, further comprising:

an insulating layer formed between the data line and one of the first pixel electrode and the second pixel electrode,

wherein the insulating layer has a dielectric constant smaller than 4.

17. (Previously presented) The electrophoretic display of claim 14,

wherein the data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti.

18. (Previously presented) The electrophoretic display of claim 14, wherein an inclination angle of the gate line or the data line relative to the surface of the substrate ranges between about 20 degrees to about 80 degrees.

19. (Previously Presented) The electrophoretic display of claim 16, wherein the insulating layer is made of a-Si:C:O or a-Si:O:F.

20. (Currently amended) An electrophoretic display comprising:

a gate line which extends in a first direction;

a data line which extends in a second direction substantially perpendicular to the first direction;

a first pixel electrode ~~overlapping one of the gate line and the data line~~ disposed in a first region restricted by the gate line and the data line;

a second pixel electrode ~~overlapping the one of the gate line and the data line~~ disposed in a second region restricted by the gate line and the data line and disposed adjacent to the first region;

a common electrode; and

a plurality of micro-capsules,

wherein each ~~of the microcapsules~~ microcapsule of the plurality of microcapsules comprises electric ink containing a plurality of color pigment particles,

wherein a color of the plurality of color pigment particles is at least one of red, green, blue, cyan, yellow, magenta, black and white, and

wherein ~~the first pixel electrode and the second pixel electrode overlap a same gate line or data line and are separated by a predetermined distance~~ one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode.

21. (Previously presented) The electrophoretic display of claim 20, wherein a portion of the first pixel electrode and a portion of the second pixel electrode overlap a portion of a width of the data line extending in the second direction between adjacent gate lines.

22. (Previously presented) The electrophoretic display of claim 20, further comprising:

an insulating layer formed between the data line and the first pixel electrode and the second pixel electrode,

wherein the insulating layer has a dielectric constant lower than 4.

23. (Canceled)

REMARKS

In response to the Office Action dated November 20, 2007, Applicants respectfully request reconsideration based on the amendments herein and the following remarks. Applicants respectfully submit that the claims as presented herein are in condition for allowance.

Claims 1-7, 9-12, 14 and 16-22 are pending in the present application. Claims 1, 2, 7, 14 and 20 have been amended. No new matter has been added by the amendments.

Applicants respectfully request reconsideration of claims 1-7, 9-12, 14 and 16-22 based upon the amendments and at least the following remarks.

Claim Rejections Under 35 U.S.C. §112

Claims 1-7, 9-12, 14 and 16-22 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement. The Examiner states that the claims contain limitations which were not described in the specification in such a way as to enable one of ordinary skill in the art to make and/or use the invention. The Examiner specifically states that the limitation "the first pixel and the second pixel electrode overlap a same gate line or a data line and are separated by a predetermined distance" in independent claims 1, 7, 14 and 20, is not supported by the disclosure in the specification as originally filed.

Referring to FIGS. 3 and 4 of the application as filed, Applicants respectfully note that a single gate line or a single data line clearly overlap two separate pixel electrodes without the two separate pixel electrodes overlapping each other. Specifically, the upper gate line 121 in FIG. 3 overlaps both the pixel electrode 191 in the center of the drawing as well as the adjacent pixel electrode (not specifically labeled) above the pixel electrode 191 in the center of the drawing. More specifically, an upper portion of the gate line 121 in FIG. 3 overlaps a lower portion of the adjacent (upper) pixel electrode, while a lower portion of the gate line 121 overlaps an upper portion of the pixel electrode 191 in the center of FIG. 3. At the same time, neither the pixel electrode 191 in the center of FIG. 3 nor the adjacent pixel electrode (not specifically labeled) above the pixel electrode 191 overlap each other. This is further illustrated in FIG. 4, wherein a

right portion (with respect to the view shown in FIG. 4) of the pixel electrode 191, i.e., the center pixel electrode 191 having the contact hole 185, overlaps a left portion of the gate line 121, while a left portion of the pixel electrode 191 immediately adjacent to and disposed to the right of the center pixel electrode 191 overlaps a right portion of the gate line 121. FIG. 4 further illustrates that neither of the aforementioned pixel electrodes 191 overlap each other. In addition, the distance between the right portion of the center pixel electrode 191 and the left portion of the adjacent pixel electrode 191 disposed immediately to the right therefrom is the predefined distance which separates the aforementioned two pixel electrodes.

Thus, Applicants respectfully submit that "the first pixel and the second pixel electrode overlap a same gate line or a data line and are separated by a predetermined distance" in independent claims 1, 7, 14 and 20 is clearly supported in at least FIGS. 3 and 4, as well as in the disclosure of the specification as originally filed.

The Examiner furthers states on page 5 of the Office action that it is "unclear how a single data line or gate line incorporates two pixel electrodes without utilizing additional data or gate lines." Applicants respectfully submit that the present invention does disclose a single data or gate line "incorporating," i.e., connecting with, two pixel electrodes. Instead, each pixel electrode is "incorporated" with an associated individual gate and data line, e.g., via the contact hole 185 connecting the pixel electrode 191 to the drain electrode 175, thereby "incorporating" the pixel electrode 191 with the gate electrode 123 (i.e., a portion of the associated gate line 121) with the associated source electrode 173 and associated data line 171, as shown in FIG. 4 of the application as filed.

Therefore, Applicants respectfully submit that independent claims 1, 7, 14 and 20 fully comply with the enablement requirement of 35 U.S.C. § 112, first paragraph.

As a result, it is respectfully requested that the rejection of claims 1-7, 9-12, 14 and 16-22 under 35 U.S.C. § 112, first paragraph, be withdrawn.

Claims 1-7, 9-12, 14 and 16-22 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. The Examiner specifically states that the limitation "the first pixel and the second pixel electrode overlap a same gate line or a data line and are separated by a predetermined distance" in independent claims 1, 7, 14 and 20, is unclear,

i.e., that it is "unclear how a single data line or gate line incorporates two pixel electrodes without utilizing additional data or gate lines," as stated on page 5 of the Office action.

As described above with respect to the rejection of claims 1-7, 9-12, 14 and 16-22 under 35 U.S.C. § 112, first paragraph, Applicants respectfully submit that the present invention does disclose a single data or gate line "incorporating," i.e., connecting with, two pixel electrodes; rather, each pixel electrode is "incorporated" with an associated individual gate and data line. More specifically, FIGS. 3 and 4 of the application as filed clearly show that the contact hole 185 connects the pixel electrode 191 to the drain electrode 175, thereby "incorporating" the pixel electrode 191 with the gate electrode 123 (i.e., a portion of the associated gate line 121) with the associated source electrode 173 and associated data line 171.

Therefore, Applicants respectfully submit that independent claims 1, 7, 14 and 20 fully comply with the requirements of 35 U.S.C. § 112, second paragraph.

As a result, it is respectfully requested that the rejection of claims 1-7, 9-12, 14 and 16-22 under 35 U.S.C. § 112, second paragraph, be withdrawn.

Claim Rejections Under 35 U.S.C. §103

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Hasegawa et al. (U.S. Patent No. 7,173,602, hereinafter "Hasegawa") in view of Drzaic et al. (U.S. Patent No. 7,030,'412, hereinafter "Drzaic '412"). The Examiner states that Hasegawa discloses all of the elements of the abovementioned claims except, *a first pixel electrode overlapping one of the gate line and the data line; and a second pixel electrode overlapping the one of the gate line and the data line, wherein the first pixel and the second pixel electrode overlap a same gate line or data line and are separated by a predetermined distance*, which the Examiner further states is taught by Drzaic '412, primarily in FIGS. 2 and 9, column 2, lines 35-37, column 8, line 67 and column 9, lines 1-2.

Applicants respectfully submit, however, that neither Hasegawa nor Drzaic '412 teaches or suggests *a gate line which extends in a first direction; a data line which extends in a second direction substantially* ***perpendicular to the first direction****; a first pixel electrode disposed in a first region restricted by the gate line and the data line; and a second pixel electrode disposed in a second region restricted by the gate line and the data line and disposed adjacent to the first*

*region, wherein one of **the** gate line and **the** data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode **and** a portion of the second pixel electrode*, as in amended independent claim 14.

Specifically, referring to FIGS. 2 and 4A of Drzaic '412, Applicants respectfully note that Drzaic '412 teaches gate lines and data lines which extend in first and second directions, respectively. See, for example, gate lines 36 and 46 (FIG. 2) and gate line 36' (FIG. 4A), as well as data lines 30 and 32 (FIG. 2) and data lines 30' and 36' (FIG. 4A). Thus, as shown in FIGS. 2 and 4A, the gate lines of Drzaic' 412 extend in a first direction, i.e., a horizontal direction as viewed in FIGS. 2 and 4A, while the data lines of Drzaic '412 extend in a second direction perpendicular to the first direction, i.e., a vertical direction as viewed in FIGS. 2 and 4A. Thus, as shown in FIGS. 2 and 4A of Drzaic, neither the gate lines extending in the first direction nor the data lines extending in the second direction overlap portions of both a first pixel electrode and a second pixel electrode.

Further, while the Examiner correctly notes that a capacitor 92' is shown extending from the gate line 36' in FIG. 4A of Drzaic '412, Applicants respectfully submit that the capacitor 92' is separate from the gate line 36' and, in particular, actually extends away from the gate line 36'. More specifically, the capacitor 92' is formed by extending a separate portion of the gate line 36' in the second direction, perpendicular to the first direction in which the gate line 36' itself extends. Likewise, gate electrodes are formed in the same manner, i.e., still referring to FIGS. 2 and 4A of Drzaic '412, the gate electrodes shown therein are formed by a separate portion of the gate line 36' which extends away, i.e., in the second direction, from the gate line 36'. As a result, no portion of the gate lines extending in the first direction overlaps any portions of any pixels in Drzaic '412. In addition, no portion of the data lines, extending in any direction, overlaps any portions of any pixels in Drzaic '412.

In contrast and in accordance with the present invention, portions of a same gate line and/or a same data line extending in the first and/or second direction, respectively, overlap both a first pixel and a second pixel, as shown at least in FIGS. 3, 7, 9 and 11 of the instant application as filed.

Thus, neither Hasegawa nor Drzaic '412 teaches or suggests *a gate line which extends in a first direction; a data line which extends in a second direction substantially **perpendicular to the first direction**; a first pixel electrode disposed in a first region restricted by the gate line and*

the data line; and a second pixel electrode disposed in a second region restricted by the gate line and the data line and disposed adjacent to the first region, wherein one of ***the*** *gate line [which extends* ***in the first direction****] and* ***the*** *data line [which extends in the* ***second direction****] is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode* ***and*** *a portion of the second pixel electrode*, as in amended independent claim 14

Thus, it is respectfully submitted that amended independent claim 14, including claims depending therefrom, i.e., claims 16-19, define over the cited references.

In addition, Applicants respectfully disagree with the Examiner's allegation that it would have been obvious, based on the symmetry of the pixels disclosed in Drzaic '412, to extend a portion of a given pixel over the pixel's respective gate line in addition to extending the pixel over a preceding gate line, as taught in FIG. 9 of Drzaic '412. Drzaic '412 teaches forming a substrate capacitor (component 92 of FIG. 9) "simply by extending the pixel electrode 94 over the preceding gate line 53" (column 9, lines 1-2). The motivation to extend the pixel of Drzaic '412 was to form the substrate capacitor and, more specifically, to form the substrate capacitor in a simple manner. Further, Drzaic '412 does not teach or suggest extending the pixel for the reason that the pixels are identical and symmetric, e.g., because it would be physically possible to extend the pixels, as the Examiner has apparently alleged. Rather, Drzaic '412 teaches away from extending the pixel in more than one direction, as to do so would be unnecessary and thus would be overly complicated for the clearly articulated reason of extending the pixel to form a substrate capacitor; there simply is no motivation in Drzaic '412 to extend the pixel in more than one direction.

Thus, neither Hasegawa nor Drzaic '412, either alone or in combination, teach or suggest *a gate line which extends in a first direction; a data line which extends in a second direction substantially* ***perpendicular to the first direction****; a first pixel electrode disposed in a first region restricted by the gate line and the data line; and a second pixel electrode disposed in a second region restricted by the gate line and the data line and disposed adjacent to the first region, wherein one of* ***the*** *gate line [which extends* ***in the first direction****] and* ***the*** *data line [which extends in the* ***second direction****] is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode* ***and*** *a portion of the second pixel electrode*, as recited in amended independent claim 14.

Thus, it is respectfully submitted that amended independent claim 14, including claims depending therefrom, i.e., claims 16-19, define over the cited references, for this additional reason as well.

Accordingly, it is respectfully requested that the rejection of claim 14 under 35 U.S.C. 103(a) be withdrawn.

Claims 1, 2, 5, 20 and 21 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Amundson et al. (U.S. Patent No. 6,545,291, hereinafter "Amundson") in view of Drzaic '412. The Examiner states that Amundson discloses all of the elements of claim 1 except *two pixel electrodes as a first pixel electrode and a second pixel electrode such that the first pixel electrode and the second pixel electrode overlap a same gate line or data line and are separated by a predetermined distance*, which the Examiner further states is disclosed primarily in FIG. 9 and column 2, lines 35-37, column 8, line 67 and column 9, lines 1 and 2 of Drzaic. The Examiner further states that Amundson discloses all of the elements of claim 20 except *a second pixel overlapping the one of gate line and the data line*, which the Examiner states is also disclosed primarily in FIG. 9 and column 2, lines 35-37, column 8, line 67 and column 9, lines 1 and 2 of Drzaic '412.

Regarding claim 1, the Examiner specifically states on pages 8-9 of the Office action that "Amundson teaches…a first pixel electrode overlapping [] one of [the] gate line and [the] data line (col. 2, lines 54-58…and Fig. 5a (330, 320) … [and] a second pixel electrode overlapping the one of [the] gate line and the data line ((col. 2, lines 54-58, Fig. 5a (330, 320)…)" (emphasis added). Applicants respectfully note that, despite the allegation in the foregoing statement of Amundson teaching "a second pixel electrode," that Amundson neither teaches nor suggests a second pixel electrode. Specifically, the Examiner's statement itself supports this contention, as the component labels of the first pixel electrode and the alleged second pixel electrode referred to therein are the same, i.e., the single pixel electrode 320 in FIG. 5a of Amundson. Further, referring to FIG. 5a, it can be clearly seen that only one pixel electrode 320 is present.

Regardless, Applicants respectfully submit that neither Amundson nor Drzaic '412, alone or in combination, teach or suggest *a gate line which extends in a first direction; a data line which extends in a second direction substantially perpendicular to the first direction; a first pixel electrode disposed in a first region restricted by the gate line and the data line; and a second*

pixel electrode disposed in a second region restricted by the gate line and the data line and disposed adjacent to the first region, wherein one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode, as in amended independent claim 1 and in similarly-amended independent claim 20.

More specifically, as described above in greater detail with respect to the rejection of claim 14, no portion of the gate lines extending in the first direction overlap any portions of any pixels in Drzaic '412, while no portion of the data lines, extending in any direction, overlap any portions of any pixels in Drzaic '412. In contrast and in accordance with the present invention, portions of a same gate line and/or a same data line extending in the first and/or second direction, respectively, overlap both a first pixel and a second pixel, as shown at least in FIGS. 3, 7, 9 and 11 of the instant application as filed.

Thus, both Amundson and Drzaic '412, alone or in combination, fail to teach or suggest *a gate line which extends in a **first** direction; a data line which extends in a **second** direction substantially perpendicular to the first direction; a first pixel electrode disposed in a first region restricted by the gate line and the data line; and a second pixel electrode disposed in a second region restricted by the gate line and the data line and disposed adjacent to the first region, wherein one of **the gate line [which extends in the first direction] and the data line [which extends in the first direction** is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode*, as recited in amended independent claim 1.

Likewise with regard to amended independent claim 20, Applicants respectfully submit that Amundson and Drzaic '412, individually or in combination, fail to teach or suggest *wherein one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode*, as in amended independent claim 20.

Thus, it is respectfully submitted that amended independent claims 1 and 20, including claims depending therefrom, i.e., claims 2-6 and 21-22 define over the cited references.

Accordingly, it is respectfully requested that the rejection of claims 1, 2, 5, 20 and 21 under 35 U.S.C. 103(a) be withdrawn.

Claims 7 and 11 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Drzaic (U.S. Patent No. 6,518,949, hereinafter "Drzaic '949") in view of Drzaic '412. The Examiner states that Drzaic '949 discloses all of the elements of the abovementioned claims except, *a first pixel electrode overlapping one of the gate line and the data line; and a second pixel electrode overlapping the one of the gate line and the data line, wherein the first pixel and the second pixel electrode overlap a same gate line or data line and are separated by a predetermined distance*, which the Examiner further states is disclosed primarily in FIG. 9 and column 2, lines 35-37, column 8, line 67 and column 9, lines 1 and 2 of Drzaic '412.

Regarding independent claim 7, Applicants respectfully submit that Drzaic '949 and Drzaic '412, either alone or in combination, fail to teach or suggest *a gate line which extends in a first direction; a data line which extends in a second direction substantially perpendicular to the first direction; a first pixel electrode disposed over [a] first thin film transistor; and a second pixel electrode disposed over [a] second thin film transistor, wherein one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode*, as recited in amended independent claim 7.

Specifically, as described above in greater detail with respect to the rejection of claims 1, 14, and 20, no portion of the gate lines extending in the first direction overlap any portions of any pixels in Drzaic '412, while no portion of the data lines, extending in any direction, overlap any portions of any pixels in Drzaic '412. In contrast and in accordance with the present invention, portions of a same gate line and/or a same data line extending in the first and/or second direction, respectively, overlap both a first pixel and a second pixel, as shown at least in FIGS. 3, 7, 9 and 11 of the instant application as filed.

Thus, it is respectfully submitted that amended independent claim 7, including claims depending therefrom, i.e., claims 9-12, define over the cited references.

Accordingly, it is respectfully requested that the rejection of claims 7 and 11 under 35 U.S.C. 103(a) be withdrawn.

Claims 3, 6 and 22 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Amundson in view of Drzaic '412 and further in view of Yamamoto et al. (U.S. Patent No. 6,563,260, hereinafter "Yamamoto"). The Examiner states that Amundson in

view of Drzaic discloses all of the elements of the abovementioned claims except, *the insulating layer having a dielectric constant lower than 4, with the insulating layer being made of a-Si:C:0 or a-Si:0:F*, which the Examiner further states is disclosed primarily in FIG. 3, column 13, lines 59-64 and column 13, lines 48-50 of Yamamoto.

Independent claims 1 and 20, from which claims 3, 6 and 22 depend, is submitted as being allowable for defining over Amundson in view of Drzaic '412 as discussed above. Furthermore, it is respectfully submitted that *the insulating layer having a dielectric constant lower than 4, with the insulating layer being made of a-Si:C:0 or a-Si:0:F* allegedly taught by Yamamoto or any other disclosure of Yamamoto does not cure the deficiency noted above with respect to Amundson in view of Drzaic '412.

Thus, it is respectfully submitted that claims 3, 6 and 22 are patentable over the cited references.

Accordingly, it is respectfully requested that the rejection of claims 3, 6 and 22 under 35 U.S.C. 103(a) be withdrawn.

Claim 4 stands rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Amundson in view of Drzaic '412 and further in view of Izumi et al. (U.S. Patent No. 7,148,867, hereinafter "Izumi"). The Examiner states that Amundson in view of Drzaic discloses all of the elements of claim 4 except, *the data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti*, which the Examiner further states is disclosed primarily in FIG. 1B, column 8, lines 10-13 of Izumi.

Independent claim 1, from which claim 4 depends, is submitted as being allowable for defining over Amundson in view of Drzaic '412 as discussed above. Furthermore, it is respectfully submitted that *the data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti* allegedly taught by Izumi or any other disclosure of Izumi does not cure the deficiency noted above with respect to Amundson in view of Drzaic '412.

Thus, it is respectfully submitted that claim 4 is patentable over the cited references.

Accordingly, it is respectfully requested that the rejection of claim 4 under 35 U.S.C. 103(a) be withdrawn.

Claims 9 and 12 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Drzaic '949 in view of Drzaic '412 and further in view of Yamamoto. The Examiner states that Drzaic '949 in view of Drzaic discloses all of the elements of the abovementioned claims except, *the insulating layer having a dielectric constant smaller than 4 with the insulating layer being made of a-Si:C:0 or a-Si:0:F*, which the Examiner further states is disclosed primarily in FIG. 3, column 13, lines 59-64 and column 13, lines 48-50 of Yamamoto.

Independent claim 7, from which claims 9 and 12 depend, is submitted as being allowable for defining over Drzaic '949 in view of Drzaic '412 as discussed above. Furthermore, it is respectfully submitted that *the insulating layer having a dielectric constant smaller than 4 with the insulating layer being made of a-Si:C:0 or a-Si:0:F* allegedly taught by Yamamoto or any other disclosure of Yamamoto does not cure the deficiency noted above with respect to Drzaic '949 in view of Drzaic '412.

Thus, it is respectfully submitted that claims 9 and 12 are patentable over the cited references.

Accordingly, it is respectfully requested that the rejection of claims 9 and 12 under 35 U.S.C. 103(a) be withdrawn.

Claim 10 stands rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Drzaic '949 in view of Drzaic '412 and further in view of Izumi. The Examiner states that Drzaic in view of Drzaic discloses all of the elements of claim 10 except, *the data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti*, which the Examiner further states is disclosed primarily in FIG. 1B, column 8, lines 10-13 of Izumi.

Independent claim 7, from which claim 10 depends, is submitted as being allowable for defining over Drzaic '949 in view of Drzaic '412 as discussed above. Furthermore, it is respectfully submitted that *the data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti* allegedly taught by Izumi or any other disclosure of Izumi does not cure the deficiency noted above with respect to Drzaic '949 in view of Drzaic '412.

Thus, it is respectfully submitted that claim 10 is patentable over the cited references.

Accordingly, it is respectfully requested that the rejection of claim 10 under 35 U.S.C. 103(a) be withdrawn.

Claims 16 and 19 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Hasegawa in view of Drzaic '412 and further in view of Yamamoto. The Examiner states that Hasegawa in view of Drzaic discloses all of the elements of claims 16 and 19 except, *the insulating layer has a dielectric constant smaller than 4*, which The Examiner further states is disclosed primarily in FIG. 3, column 9, lines 9-19 and column 13, lines 59-64 of Yamamoto.

Independent claim 14, from which claims 16 and 19 depend, is submitted as being allowable for defining over Hasegawa in view of Drzaic '412 as discussed above. Furthermore, it is respectfully submitted that *the insulating layer has a dielectric constant smaller than 4* allegedly taught by Yamamoto or any other disclosure of Yamamoto does not cure the deficiency noted above with respect to Hasegawa in view of Drzaic '412.

Thus, it is respectfully submitted that claims 16 and 19 are patentable over the cited references.

Accordingly, it is respectfully requested that the rejection of claims 16 and 19 under 35 U.S.C. 103(a) be withdrawn.

Claim 17 stands rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Hasegawa in view of Drzaic '412 and further in view of Izumi. The Examiner states that Hasegawa in view of Drzaic discloses all of the elements of claim 17 except, *the data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti*, which the Examiner further states is disclosed primarily in FIG. 1B, column 8, lines 10-13 of Izumi.

Independent claim 14, from which claim 17 depends, is submitted as being allowable for defining over Hasegawa in view of Drzaic '412 as discussed above. Furthermore, it is respectfully submitted that *the data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti* allegedly taught by Izumi or any other disclosure of Izumi does not cure the deficiency noted above with respect to Hasegawa in view of Drzaic '412.

Thus, it is respectfully submitted that claim 17 is patentable over the cited references.

Accordingly, it is respectfully requested that the rejection of claim 17 under 35 U.S.C. 103(a) be withdrawn.

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Hasegawa in view of Drzaic '412 and further in view of Hirota. The Examiner states that

Hasegawa in view of Drzaic '412 discloses all of the elements of claim 18 except, *the inclination angle of the gate line or the data line relative to the surface of the substrate ranges between about 20 degrees to about 80 degrees*, which the Examiner further states is disclosed primarily in FIG. 5, column 5, lines 28-34 and 65-67 of Hirota.

Independent claim 14, from which claim 18 depends, is submitted as being allowable for defining over Hasegawa in view of Drzaic '412 as discussed above. Furthermore, it is respectfully submitted that *the inclination angle of the gate line or the data line relative to the surface of the substrate ranges between about 20 degrees to about 80 degrees* allegedly taught by Hirota or any other disclosure of Hirota does not cure the deficiency noted above with respect to Hasegawa in view of Drzaic '412.

Thus, it is respectfully submitted that claim 18 is patentable over the cited references.

Accordingly, it is respectfully requested that the rejection of claim 18 under 35 U.S.C. 103(a) be withdrawn.

Conclusion

In view of the foregoing remarks distinguishing the prior art of record, Applicants submit that this application is in condition for allowance. Early notification to this effect is requested. The Examiner is invited to contact Applicants' Attorneys at the below-listed telephone number regarding this Amendment or otherwise regarding the present application in order to address any questions or remaining issues concerning the same. If there are any charges due in connection with this response, please charge them to Deposit Account 06-1130.

Respectfully submitted,

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